The MPEG Single Channel Transport Stream De-multiplexer is designed to cater to various broadcast and professional video applications. The transport stream is specified in MPEG-2 Part 1 – Systems and is compliant with ISO/IEC 13818-1 standard. It is also known as ITU-T H.222.0. The demultiplexer takes in the AV input stream and separates out the audio and video content as respective elementary stream for further processing by respective decoders.

The TS-Demux solution is available in both FPGA Netlist and Source Code licensing models. CoreEL can also customize the core according to end application requirements.

The TS-Demux module includes the basic components needed for transport stream de-multiplexing as shown in block diagram. The TS-Demux process is categorized into the following function:

- The incoming packet contains the multiplexed private, video, audio & PSI sections data, they should be properly de-multiplexed on to designated ports
- The PSI and Adaptation data are forwarded to host
- The video and audio are properly transferred to respective ports

### Key Features

- ISO/IEC 13818-1 MPEG-2 Transport Stream compliant
- Single Channel 1-bit serial or 8-bit parallel compile option input interface support
- Support up to 64 PID, PES/PSI section filtering
- Single/Multiple agent support for output ports
- Sync detection for 188/104/208 bytes packet
- Support for CRC checksum
- Support three 8-bit output port – Video, Audio & Private data
- Supports external de-scrambling interface
- Single/Multiple PCR PID Filtering Support
- Maximum input data rate support up to 216Mbps
- Support for MPEG-2 measurement statistics
- Provides Host interface to PSI Section and Adaptation data
- Configurable Output format PES/ES

### Block Diagram
Transport Stream De-multiplexer

Configurable Features
Many features of TS-Demux can be configured during the operation of de-multiplexer. The features that can be configured include:
- Video/Audio stream ID filter
- Output stream format
- PID filtering table

The features that can be configured during the synthesis time include:
- Input interface data width
- Custom stream ID filtering
- PCR PID filtering for different agents
- CRC implementation

Resource Utilization

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<th>Xilinx 5/6/7 Series Devices</th>
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Deliverables
The netlist version of the core comes with:
- EDIF (or) NGC netlist
- Implementation scripts and constraints
- TS-Demux User Manual

The deliverables for full source code license are:
- Verilog source files
- Comprehensive test bench
- Scripts to run simulation
- Test case reports
- Design Document
- User Manual
- Implementation scripts and constraints

Application
- Broadcast and Professional decoders
- Integrated receiver decoders
- Broadband communications
- Test and Measurements

About Us
CoreEL Technologies is a Customer Application Specific Product & Solutions (CASPS) company offering innovative solutions from its diverse portfolio of expertise that includes Intellectual Property (IP) cores, system design, manufacturing, sustenance and OEM solutions in the form of EDA tools, Mechanical Engineering tools, COTS products and Technology Training. CoreEL’s strength lies in its ability to blend deep domain knowledge with the right ingredients across its portfolio of offerings. It is a leading developer of advanced electronic system level products and solutions to three primary markets - Aerospace & Defence, Digital Media Broadcast, and Universities and Institutions of Higher Learning.