Multi-bit Digital Receiver based on FPGA for Real time Pulse Detection and Parameter Measurement for EW

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Abstract- This paper brings out a unique FPGA based Pulse detection and characterization approach for a Digital ESM (Electronic Support Measure). The proposed approach uses a high speed ADC and FPGA based architecture for sampling and Digital processing of the received RADAR signals.

Key Words- EW, ESM, Digital Receiver, FPGA, Band pass Sampling, High Speed FFT, Peak Detection, Frequency Domain Blanking, NCO, Tunable LPF, Envelope Detection, Arctangent Computation, Pulse Description Words

I. INTRODUCTION

An earlier paper[1] had discussed the need for ESM receivers, advantages of using digital techniques for realization of the ESM receivers and challenges involved in their realization. It had also detailed an outline and presented the experimental results of using a hyper speed 256 point FFT engine for detecting the presence of multiple emitters and for measuring their coarse frequency using a FPGA based system. The present paper develops on it and presents the architecture of a realized Digital Receiver System. It also presents the experimental results of this system.

Ability to detect the presence of multiple emitters that overlap in time domain is becoming the need of the hour as Radar frequency spectrum is getting crowded. ESM Receivers are required to process a few million pulses/second for maintaining a high POI (Probability of Intercept).

The availability of high speed ADCs in the GHz range have made direct sampling of signals possible in the IF range. Emergence of high density/high speed FPGAs with dedicated resources for performing DSP operations has enabled implementation of ESM techniques operating in real time.

II. PULSE DETECTION ARCHITECTURE

Our earlier paper[1] had presented a choice of 1350 MHz as sampling frequency to sample band-limited signals in the range 750 MHz to 1250 MHz for its operation. Choice of 256 point hyper speed FFT engine for signal detection and measurement of coarse frequency with resolution of 5.86 MHz was made.

III. DIGITAL RECEIVER ARCHITECTURE

Fig. 1 shows the architecture of Digital Receiver System. It is a Virtex-5 SX240T FPGA based system that receives the signal conditioned RF data over 2 channels. The RF signal is band-limited signal in the range 750 MHz – 1250 MHz. High speed dual ADC chip sampling the data at 1350 MHz is employed and digitized signal samples are further processed in the FPGA. Pulse Description Words are formed and are sent to DSP processor based system for further processing.

- Dual channel ADC chip contains 2 independent high speed ADC's that samples the incoming signal at 1350 MHz to give data samples of 8-bit width. Sampling clock is generated on board. FPGA receives the data samples from ADC's over source synchronous LVDS interfaces. From each of the ADC's, 2 data interfaces operating at 337.5 MHz DDR rate provide the delayed and non-delayed data samples that correspond to 2 consecutive data samples.
- Digital Receiver FPGA is a DSP resource intensive virtex-5 FPGA from Xilinx. Digital Receiver functionality is realized on this FPGA using VHDL as the RTL language. The device is ideal for realization of DSP functionalities at high speeds as it has a flip-flop rich architecture with sufficient BRAMs.

  The RTL design is modular and functionally divided into further sub-units.

- ADC interface module programs the ADC chip through a low speed serial interface upon configuration/reset. This module also receives the source synchronous data from the ADCs and provides it to further modules for processing. It handles cross clock domain issues. Further data is viewed as 8 samples width operating at SDR rate of 168.75 MHz
- Data from the ADC interface module is viewed further as blocks of 256 samples. Each of the blocks are time

stamped for measuring the Time of Arrival of signals. The data samples are stored in the local on-board memories and also provided to Parameter Measurement and PDW Generation Block.

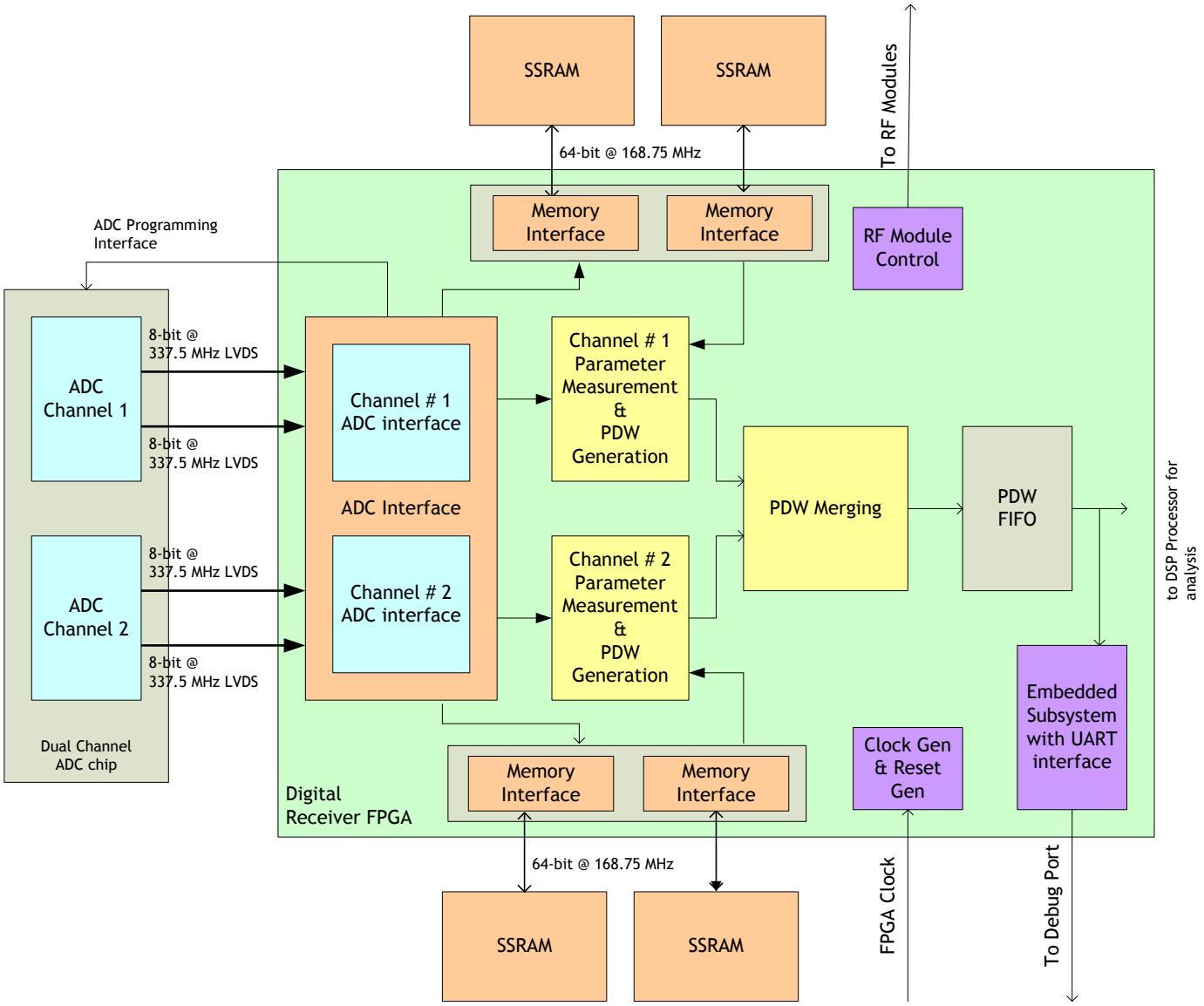

Fig. 1: System Overview of Digital Receiver

- Each data channel has dedicated memory for storing of data for further processing. 4 SSRAM memories of 4 MB storage each and 64-bit, operating at 168.75 MHz are connected to FPGA. Each channel uses 2 such memories in the ping-pong fashion for each block of data – for storing and retrieval purposes. Memories are implemented as cyclic buffers, depth of the cyclic buffer being sufficiently higher than the total processing delay within the FPGA. These memories are capable of providing sustained write/read bandwidth of 1350 Msps. FPGA implements the necessary memory interface and memory arbitration logic operating at such high speed.

- Parameter Measurement and PDW Generation module carries out all the signal processing operations. This is explained in detail in further sections.

- PDW Merging module merges like PDW's generated – so as to reduce the computational over-head on the DSP processor. At any time, about 32 unique PDWs can be considered by this module for merging. At regular intervals of time, this data is sent to DSP processor for further processing. Data is also sent whenever 33rd type of PDW is received by this module.

- RF Module control drives discrete IO signal circuitry of the RF front end. Based on the commands received from DSP processor, these signals are driven so as to tune the RF filters to select spectrum of 500 MHz, down-converted to the range 750 MHz to 1230 MHz.

- Clock Gen and Reset Gen module generates various clocks required for the operation of ADC interface, memory interface, logic modules and embedded sub-system. DCM's in the FPGA are utilized for skew management and for generation of clocks of different frequencies. Cross clock signal handling is a major challenge in this project due to high number of clocks.

- Micro-blaze based embedded sub-system developed using Xilinx's Embedded Developers' Kit (EDK) is used for configure, control and status monitoring of the Digital Receiver System. Through the UART interface, the operator can carry out all these operations.

IV. PARAMETER MEASUREMENT & PDW GENERATION

Fig. 2 shows the Parameter Measurement & PDW generation Block.

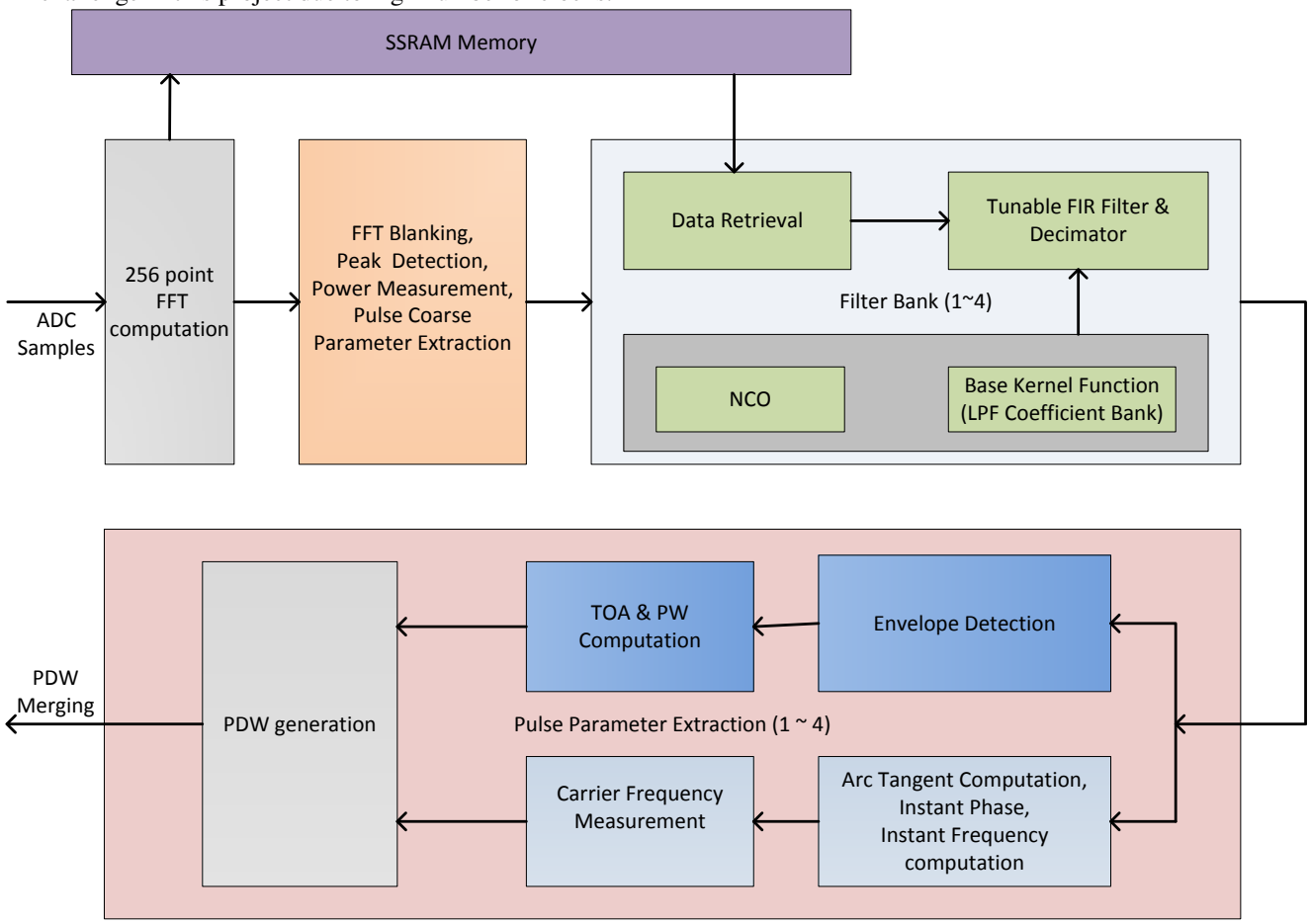

Fig. 2: Parameter Measurement & PDW Merging

- Custom designed hyper speed 256 point FFT engine capable of processing the data at 1350 MSPS is the instantiated. The data samples are windowed to reduce the effect of DFT leakage using Kaiser Window Function. Technique presented in "Understanding Digital Signal Processing"[2] is utilized to compute the FFT of 2 real sequences using single FFT engine.
- FFT bins are analyzed to detect the presence of emitters. FFT blanking feature provides the operator with facility to blank-out specific emitters/jammers from further analysis. Based on the bin strength, the strength of the emitter signal is determined, using a calibrated look-up table. Detection of weak signals in the presence of strong signals, especially for narrow width pulses, with DFT leakage coming into picture presented a great challenge to our work. Side lobe rejection mechanism was developed to handle this kind of condition. Bins are monitored and coarse frequency measurement value, coarse time of arrival and coarse pulse width information is passed on to the Filter bank module.
- Emitters are assumed to be having a bandwidth of around 5 MHz. Based on the coarse measurements, the data

samples are retrieved from the on-board memory and subjected to further processing. Low pass filter co-efficient are multiplied with sine/cosine samples being produced by an NCO to get the co-efficient for a Bandpass filter centered at measured coarse carrier frequency. Xilinx FIR filter IP core is used for filter realization and decimation. These filters are dynamically tunable with given co-efficient. When data samples are passed through this filter, I & Q versions of the signal are obtained. A decimation factor of 32 is used due to limited bandwidth of the incoming signal and this results in a great reduction of data throughput for further modules.

4 instances of NCO and Dynamic tunable FIR decimator are used for each data channel so as to detect upto 4 over-lapping emitters at any given point of time.

- Pulse Parameter Extraction module has 4 independent signal processing paths for characterization of 4 emitter signals. Using envelope detector technique, Pulse width of the signal is computed. Interpolation technique using the properties of similar triangles enables to compute the pulse width and time of arrival of the signals with greater resolution from decimated sample values. Note that a 100 ns wide signal after decimation gives only about 4 samples, from which Pulse width and Time of arrival has to be calculated.
  Parallely, from I and Q versions of the data samples, auto-correlated versions of I & Q data samples are calculated. Instantaneous phase of the signal is calculated followed by instantaneous frequency calculations. All computations are carried out in fixed binary point format as implementation of floating point operations in FPGA's is a very expensive affair. Arc tangent function is complex function to realize in hardware. Approach of CORDIC was not suitable for this application as it is an iterative algorithm and data needs to be processed in pipeline for this architecture. We chose an approach presented in "Understanding Digital Signal Processing"[2]. Throughout the pulse width period, the instantaneous frequencies are accumulated and divided by pulse width to get the carrier frequency. In case there are abrupt changes in the instantaneous phase, it points to coded modulation – such as use of Barker codes.
- Assembling computed values from various modules, a Pulse Description Word is formed. A typical PDW will have the following parameters: carrier frequency, Pulse arrival time, Pulse Width, Strength of the emitter in dB, type of modulation and channel number.

V. FPGA RESOURCE UTILISATION

RESOURCE UTILIZATION	
Device	XC5VSX 240T -1
Clocks in MHz	337.5, 168.75, 50
FF utilization	71%
BRAM utilization	58%
DSP utilization	41%
Slice Utilization	97%

VI. SYSTEM PERFORMANCE

The Digital Receiver system was extensively tested and validated for different scenarios in the lab using a Threat Simulator system. The generated PDWs were analyzed following results were noted:

PARAMETER & ACCURACY	
Dynamic Range	35 dB
Pulse Amplitude	0.5 dBm
Carrier Frequency	1 MHz
Pulse Width	25 ns for minimum pulse width of 100 ns with lowest strength
Time of Arrival	25 ns for minimum pulse width of 100 ns with lowest strength
Modulation on Pulse	Fixed Frequency, Coded & Modulated
Number of PDWs	2.5 million pulses per second
Number of simultaneous emitters	Upto 4

X. CONCLUSIONS

Digital Receiver system has been tested extensively in the lab using Threat Simulator for different scenarios and the results have met the design specifications in terms of functionality and throughput requirements. This holds a great promise for future DR systems for ESM applications.

Xilinx Virtex-5 SX FPGAs have proven to be a success for Digital Receiver applications, both in processing performance and in I/O bandwidth for signal processing and data communications. The release of Virtex-7 family and especially the Zync series with ARM processors holds greater scope for improvements and enhanced capabilities due to even faster data rates, higher processing resources and lower power consumption. The embedded ARM processors can take up the additional functionality of de-interleaving and classification of emitters – further reducing the size of the system – especially suited for airborne applications. This would also result in lesser expensive solutions for design and manufacture. In terms of signal processing capabilities, Digital Receiver system can further be augmented with additional signal processing modules such as Direction Finding algorithms.

Availability of higher resolution ADCs such as 10-bit and 12-bit resolution, capable of sampling the signals at 1350 MHz holds greater promise for achieving better dynamic range. Due to Technology advancements in the ADC's, it has now become possible to procure ADCs capable of sampling at frequencies as high as 3000 MHz. This along with emergence of high density high speed FPGAs, holds promise for design and development of DR systems capable of surveying upto 1000 MHz spectrum at any given point of time.

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