FPGA based System implementation of Scalable Digital Beam Forming Unit for RADAR Applications

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***Abstract*- This paper brings out a unique method of implementing FPGA based Scalable Digital Beam Forming Unit that can be used for RADAR applications. The proposed approach uses multi-FPGA, multi-card solution for realizing Digital Beam forming functionality that can be used to synthesize multiple digital beams with data received from multiple Receivers. Processors available as hard macros within the FPGAs are used to configure, control and monitor the operations.**

***Key Words*- Digital Beam Forming, Field Programmable Gate Arrays (FPGA), Radar Environment Simulation, Management Information Base, Dynamic Weights, Gigabit Transceivers, Remote configuration, Scalability, Testability, Modular Approach**

I. INTRODUCTION

Digital Beam forming enables synthesis of simultaneous multiple beams. As the need for building high range RADARs with high directivity is increasing day by day, computational requirements to process the data from increased number of receivers is also growing. Modern day high density FPGAs are best suited for implementing these functionalities as they provide very high computational bandwidth. Traditional RADARs have used analog techniques to synthesize the beams. Use of digital techniques in beam formation will enhance the flexibility and overcome multiple issues that are present in analog systems. Previously DBF functionality has been implemented for ultra-sound and mobile communication domains.

In this paper, we bring out design and implementation approach of Scalable Digital Beam Forming Unit (henceforth DBF) for RADAR applications. The paper also reports how the design was partitioned into hardware, software, mechanical and RTL components.

II. STATEMENT OF PROBLEM

RADARs with high directivity and range involve reception and processing of data from very high number of receiver elements. A RADAR RF front end unit with multiple sensors/receivers of the order of thousands was conceptualized based on system requirements. In the scheme, received signals from a few of sensors were combined using power combiners and then passed through ADCs. Digitised data was subjected to complex decimation, effectively reducing the data rates to a few MSPS. Data samples from 8 ADCs were multiplexed and with appropriate packet headers, delivered to DBF unit via optical interfaces for further processing. This resulted in 60 data links on which received data gets delivered to DBF.

DBF has to accept the data through these links, synthesize 12 beams and deliver this data to Signal Processing Units for further processing. DBF should communicate the data with Signal Processing Units over links with sFPDP protocol. Configuration, Control and Status monitoring of the DBF unit through Ethernet as well as a control link with sFPDP protocol should be supported. Design of DBF should be modular, scalable and should include features for observability and testability.

III. SYSTEM DESCRIPTION

Complex digitized samples from the receivers are multiplied with complex beam weights and are summed to get single or multiple beams of data.

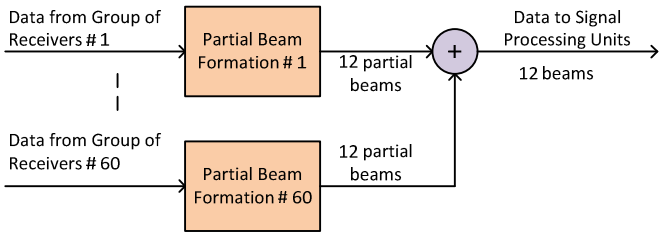

Fig. 1: DBF Functional Overview

Multiplexed complex data of 16-bit in-phase and quadrature phase on 60 links at 5 Msps rate from 8 ADCs would translate to incoming data rate of as high as 76.8 Gbps. Synthesis of 12 beams of data would translate to more than 250 Giga operations / second. Virtex-5 generation of Xilinx FPGAs provide an excellent balance of I/O bandwidth to computational capacity and are well suited for repetitive parallel operations such as beam formation. They provide more compact and economical solution compared to high performance computing Processor based approach. Hence FPGA based system was conceptualized.

Keeping in view the limitations in terms of physical dimensions of the card, thermal management challenges, FPGA high speed serial link resources and desire for modularity and scalability, the system was designed to be a multi-card, multi-FPGA solution. FX flavor of FPGAs with in-built Power PC processor hard macro were chosen and in each of the FPGAs embedded processor sub-systems were created. This provided the system with enormous flexibility

and programmability and the software ported on these processors carried out one-time configurations, controls and continuous status monitoring operations.

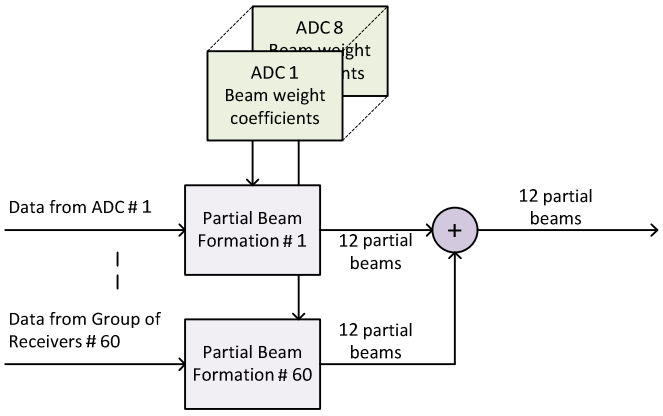

Fig. 2: Partial Beam Formation in DBF

IV. Digital Beam Former Design

DBF System consists of 2 types of data processing cards viz., Intermediate Digital Beam Former (IDBF) Card and Final Digital Beam Former (FDBF) Card.

Each IDBF card is interfaced to 12 optical links and can receive data from 12 Group of Receivers. IDBF Card consists of 2 types of FPGAs, First Level Beam Former (FLBF) and Intermediate Level Beam Former (ILBF). There are 3 FLBF's, each catering to processing needs of 4 Group of Receivers. Partial Beam data is transferred from FLBF to ILBF via on board high speed serial links. Data from ILBF is transferred to FDBF card optical interface.

FDBF card consists of a single FPGA that receives partial beams from upto 5 IDBFs. FDBF card provides Ethernet connectivity with external world. FDBF has 2 sets of 3 optical links each for interfacing with Signal Processing Units for further processing of data. There is a dedicated optical link over which commands are received at FDBF for further processing. FDBF acts as the system master controlling power sequencing, reset sequencing, FPGA configuration sequencing and POST operations.

Along with System Monitor primitive present in the FPGAs, on board sensors for measuring temperature, voltage levels, humidity etc., are provided as part of system status monitoring.

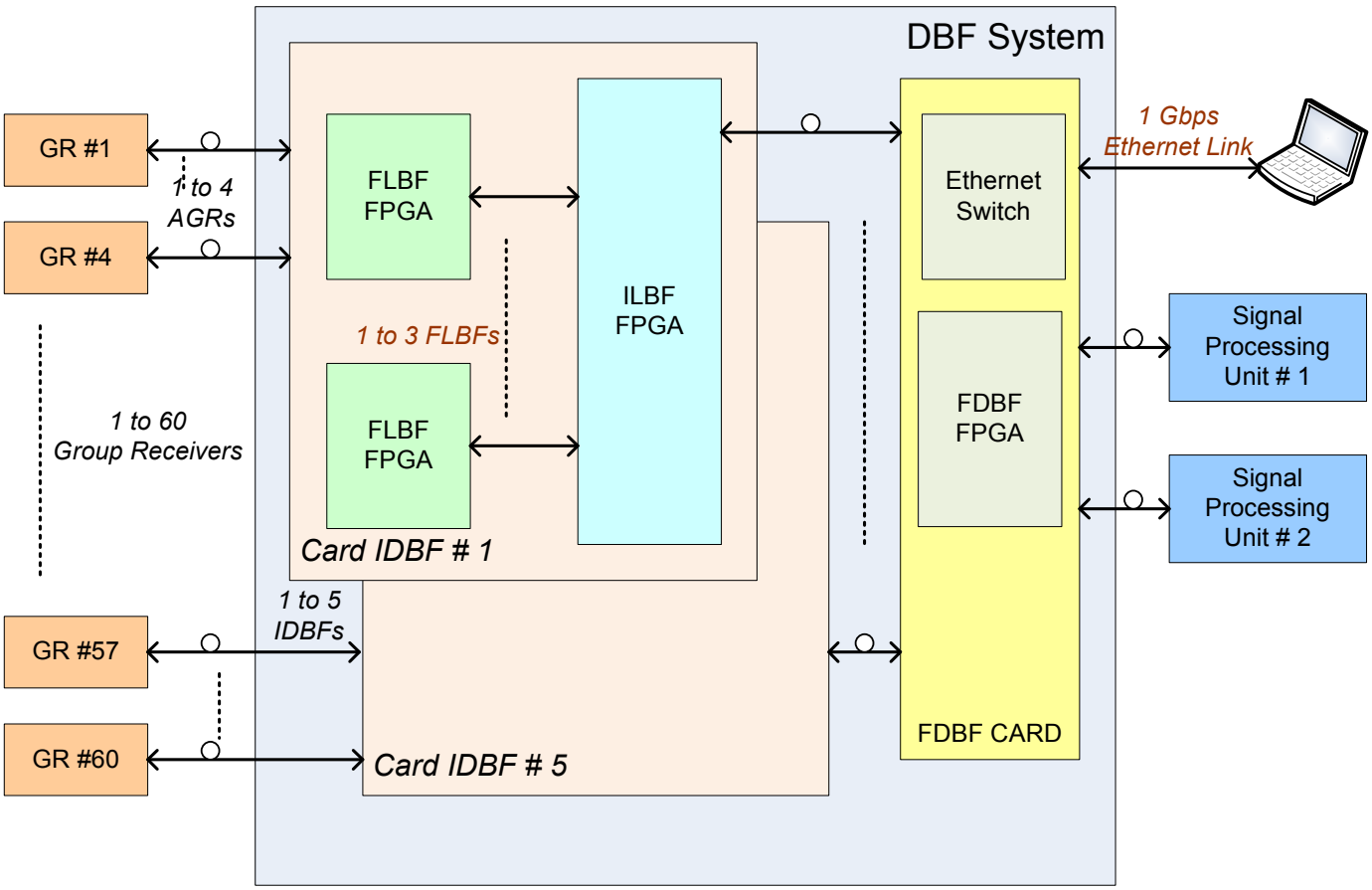

Fig. 3: System Overview of DBF

V. DATA ACQUISITION, TRANSFER & DELIVERY

The gigabit transceivers available in the FPGAs have been used extensively for high speed serial communication. Multiplexed data samples from Group of Receivers are received in the form of packets over the optical interface at FLBF FPGA. Aurora Protocol, a link-layer, scalable, light-weight open protocol from Xilinx is used for this communication. Group of Receivers communicate at 3.6 Gbps with FLBF over optical links. System wide generic message structure for communicating messages in the form of packets was developed with header fields incorporating features of well established protocols such as Ethernet.

FLBF transfers the partial beam data to ILBF over on-board high speed serial links using Aurora protocol at 7.2 Gbps. Channel bonding feature of the Aurora protocol is used to bond 2 links operating at 3.6 Gbps as a single channel for data transfer.

FDBF transfers the final beam data over 2 sets of 3 optical links each to Signal Processing Units for further data processing. sFPDP protocol operating at 2.5 Gbps has been used for this communication.

Though the data flow is majorly from Group of Receivers to Signal Processing Units, periodic control and configuration messages flow in the reverse direction. Hence all the links are duplex channels.

VI. SYNTHESIS OF BEAMS

Complex Beam weight coefficients are programmed in Flash memories present on IDBF cards. Based on the geographical ID learnt through backplane, the ILBF programs the FLBFs with relevant coefficients.

Data packets from the Group of receivers are received at regular intervals at FLBF FPGAs. Packets arriving within a time window with same packet id and burst id are considered for further processing, while packets arriving out of this window and with wrong parameters are dropped and information is logged. I&Q data in fixed point binary format is converted into floating point format for further processing. Processing in floating point format provides higher dynamic range for representing numbers and addresses the issue of bit growth. However, the implementation of floating point arithmetic units in FPGAs is resource intensive, in comparison to fixed point arithmetic. Complex data samples from each of the ADCs are multiplied with corresponding complex weights to form 12 partial beams. Data samples belonging to a partial beam are added with corresponding data samples first at ADC level in FLBF FPGA and then at Receiver Unit level at ILBF and FDBF.

DBF also implements Radar Environment Simulation module. Multiple virtual threats can be generated and super-imposed on data being received in real time. User sends information regarding time of appearance of threat, their duration, Doppler effect parameters, relative attenuations among synthesized beams etc., and creates these threats. Using this feature, Signal processing Units can independently be validated during system integration phase.

Beam forming technique is BRAM and DSP48 resource intensive. As the floating point arithmetic is expensive in terms of FPGA resources, the resources need to be time shared for carrying out operations. This means that entire logic has to operate at higher speeds. RTL design and coding has to take into account High speed design guidelines and practices to ensure that design meets functionality as well as performance requirements in one go. As the design involves multiple modules operating wrt different clocks, due care has to be taken to address cross-clock domain issues in FPGA. RTL also implements various statistics counters, sticky bits and other in-built debug and status monitoring options, so that when DBF is in field, status can remotely be monitored.

VII. PROCESSOR SUB-SYSTEMS

Xilinx's Virtex-5 FXT series of FPGAs come with Power PC 440 embedded processor. These embedded processors are seamlessly integrated with other essential components of an embedded sub-system such as Trimode Ethernet MAC core, dedicated DMAs, integrated crossbar, DDR memory controller etc. Using Embedded Developers' Kit from Xilinx, processor based embedded sub-system was implemented on all the FPGAs. On board facilities essential for operation of the embedded sub-systems were provided such as Flash memories, DDR2 memories, Console port, I2C EEPROM etc.

VIII. OS & APPLICATION SOFTWARE

While RTL implementation is well suited for repetitive high throughput computational tasks, it lacks the flexibility and programmability in comparison to Processor based software implementation approach. DBF like complex systems have numerous configuration, control and status monitoring tasks that are performed at regularly in a periodic manner. Power on Self Test (POST), support for observing the health of the system, remote upgradability of FPGA images, status monitoring etc. can easily be provided by the software.

Power PC based embedded sub-system and associated peripherals provide a great infrastructure for software implementation of these tasks. DBF architecture makes use of this.

IX. SYSTEM SUMMARY

Table 1: DBF System overview

Parameter	
Number of FPGAs in DBF	28
Linux running on	12 FPGAs
XILKERNEL running on	15 FPGAs
BITE implementation on	7 dedicated FPGAs
Data path frequency	180MHz
Total number of optical links	87
Optical link speed	3.6 Gbps
Number of sFPDP links	7 @ 2.5 Gbps
Number of different cards in DBF	9

Table 2: FPGA resource utilization

	FLBF	ILBF	FDBF
Device	XC5VFX 100T-1	XC5VFX 100T -1	XC5VFX 130T -1
Clocks in MHz	90,100, 125,180, 200	100, 125, 180, 200	62.5,100,125, 180,200
FF utilization	74%	39%	72%
BRAM utilization	88%	58%	94%
DSP utilization	25%	0%	45%
GTX utilization	50%	62%	90%

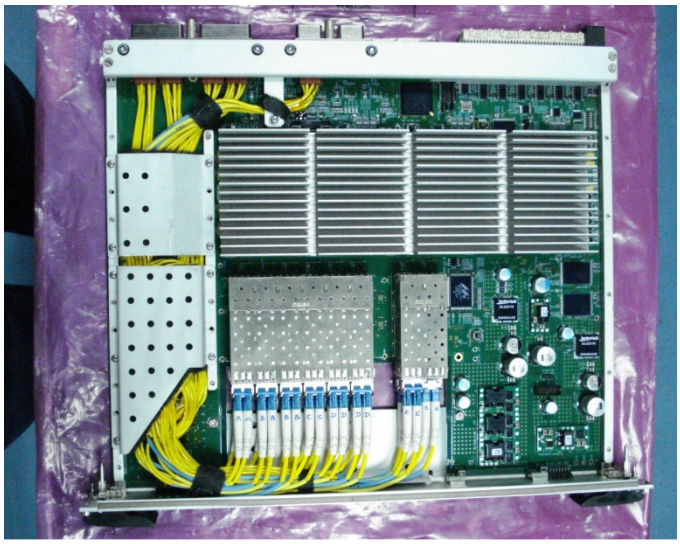

Fig. 4: IDBF card with optical cables routed. Ready to be put into mechanical enclosure. Heat sinks cover the FPGAs.

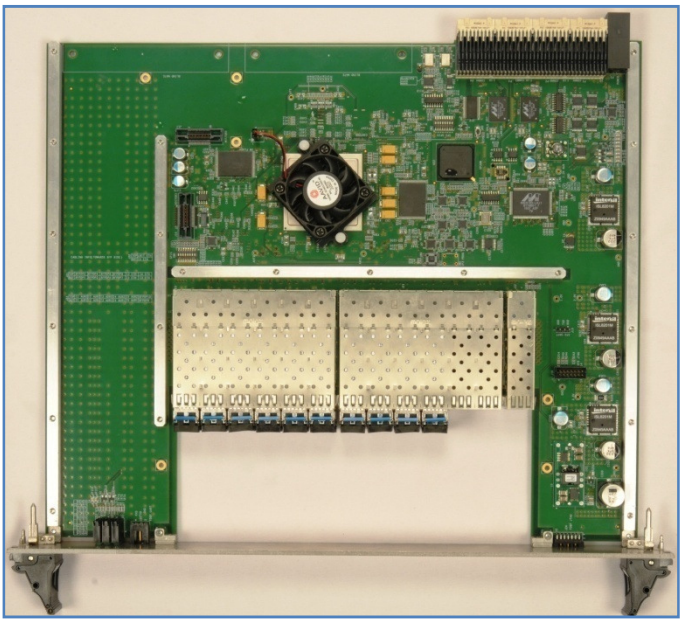

Fig. 5: FDBF card without optical cables. FPGA is mounted with active heat sink for lab testing

X. Conclusions

DBF system has been tested extensively in the lab using Automatic Test Equipment for different scenarios and the results have met the design specifications in terms of functionality and throughput requirements. This holds a great promise for future RADAR systems.

Timely and successful implementation of the DBF system that requires multi-disciplinary expertise and co-ordination among teams has been possible due to proper planning, consistent adherence to quality control and assurance processes, reviews, adoption of best engineering practices and hard work.

Xilinx Virtex-5 FPGAs have proven to be a success for DBF applications, both in processing performance and in I/O bandwidth for signal processing and data communications. The release of Virtex-7 family and especially the Zync series with ARM processors holds greater scope for improvements and enhanced capabilities due to even faster data rates, higher processing resources and lower power consumption. This would also result in lesser expensive solutions for design and manufacture. In terms of signal processing capabilities, DBF system can further be augmented with additional signal processing modules such as adaptive beam forming, signal averaging etc.

Fig. 6: DBF System with mechanical enclosure

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REFERENCES

1 Toby Haynes, *A Primer on Digital Beam Forming,* Spectrum Signal Processing

2 Abhijit Athavale and Carl Christensen, *High –speed Serial I/O made simple, A designers' Guide with FPGA Applications*, Xilinx, ed. 1

3 Reference Guide, *Embedded Processor block in Virtex-5 FPGAs*, Xilinx, v1.8

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