FPGA based Modular and Generic Automated Test Equipment (ATE) for Digital Beam Forming Unit

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***Abstract*- This paper brings out Generic and Modular architectural view of Automated Test Equipment (ATE) that is used for validating Digital Beam Former (DBF) system. The proposed approach uses multi-FPGA, multi-card solution for realizing ATE functionality that is used to completely validate DBF system. Processors available as hard macros within the FPGAs are used to configure, control and monitor the operations.**

***Key Words*- Automated Test Equipment (ATE), Digital Beam Forming, Field Programmable Gate Arrays (FPGA), Group Receivers (GR), Radar Environment Simulation (RES), Gigabit Transceivers, Remote configuration, Scalability, Signal Processor (SP), Space and Time Management Unit (STM), Testability, Modular Approach**

I. INTRODUCTION

Brief introduction to DBF: CoreEl has implemented FPGA based scalable DBF system that can be used for RADAR applications. DBF uses multi-FPGA, multi-card solution to realize Digital Beam forming functionality. DBF interfaces to up to 60 Array of multiple Receivers using Aurora protocol on optical links each operating at 3.6Gbps (totaling to aggregate raw input data bandwidth equal to ~76.8Gbps). DBF synthesizes multiple output beams and sends them to Signal Processor (SP) using sFPDP protocol on six optical links operating at 2.5Gbps (totaling to aggregate raw output data bandwidth equal to ~8Gbps). DBF also supports Radar Environment Simulator (RES) feature to simulate virtual threats. The actual bandwidth needed on optical links would be ~30% more to cater to Protocol Headers, Control Information, 8B/10B encoding, etc.

Introduction to ATE for DBF: From DBF introduction, it is clear that the performance and bandwidth needed to test DBF cannot be achieved using any off-the-shelf solutions. Neither will it be possible to off-load analyses of received data to SW as it may require a huge farm of servers. This necessitated a custom designed, flexible and modular ATE System (HW/RTL/SW). Modern day high density FPGAs containing DSP elements, embedded processor and multi-gigabit transceivers are ideally suited to design an ATE system.

In this paper, we report our design and implementation approach of Modular and Generic **A**utomated **T**est **E**quipment (ATE) for **D**igital **B**eam **F**orming (DBF).

II. STATEMENT OF PROBLEM

The primary role of an ATE is to pump stimulus data to the **D**evice **U**nder **T**est (DUT) and to analyze received data with expected data in an automated way. To make Generic and Modular ATE, following features shall also be supported:

1. ATE shall provide data to DUT at wire-speed and perform run-time analysis of received data from DUT. Implementing these features in RTL shall significantly reduce overhead on Software and increases system performance.
2. ATE shall support "logging" of result data in some memory for offline analysis/processing/plotting.
3. The design of ATE shall not be tightly coupled to DUT. In another way, ATE shall contain memories to store stimulus and result data. In this way, some offline utility can generate pre-processed stimulus and result data.
4. Design of ATE should be modular, scalable and should include features for observability and testability.
5. ATE shall support features to test itself in standalone mode (before being used to test DUT). After all, no one designs ATE for ATE.

III. SYSTEM DESCRIPTION

Keeping in mind above principle, ATE architecture and features were defined. Virtex-5 generation of Xilinx FPGAs provide an excellent balance of I/O bandwidth to computational capacity and are well suited for data processing operations. They provide more compact and economical solution compared to high performance computing Processor based approach. Hence FPGA based system was conceptualized.

Keeping in view the limitations in terms of physical dimensions of the card, thermal management challenges, FPGA high speed serial link resources and desire for modularity and scalability, the system was designed to be a multi-card, multi-FPGA solution. FX flavor of FPGAs with in-built Power PC processor hard macro were chosen and in

each of the FPGAs embedded processor sub-systems were created. This provided the system with enormous flexibility and programmability and the Linux based software ported on these processors carried out one-time configurations, controls and continuous status monitoring operations.

IV. ATE Architecture

Logical block diagram of ATE is shown in Figure 1:

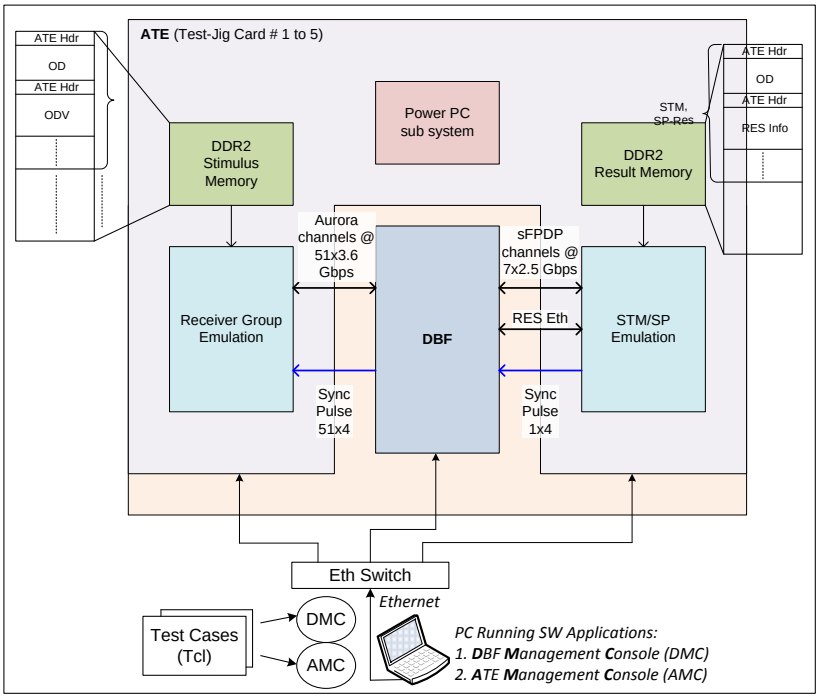

Figure 1: Logical Block Diagram of 51-GR ATE for 51-GR DBF

To validate up to 60 **G**roup **R**eceiver (GR) DBF, ATE consists of 5 Test-Jig cards. Each Test-Jig card caters for following:

1. Input data generation for up to 1 STM link operating at 2.5-Gbps following sFPDP protocol.
2. Input data generation for up to 12 Receiver Groups operating at 3.6-Gbps following Aurora protocol.
3. Input data generation for up to 1 RES link operating at 1-Gbps following Ethernet protocol.
4. Output data comparison/logging for up to 3 SP links operating at 2.5-Gbps following sFPDP protocol.

V. Test Setup for 51 GR DBF Validation

Test setup architecture for 51 GR DBF testing is depicted in Figure 2. In case of 51 GR DBF, the DBF system has 51 GRs in five rows with a per row configuration of 9, 11, 11, 11, 9 GRs. ATE emulates identical GR configurations while testing 51 GR DBF.

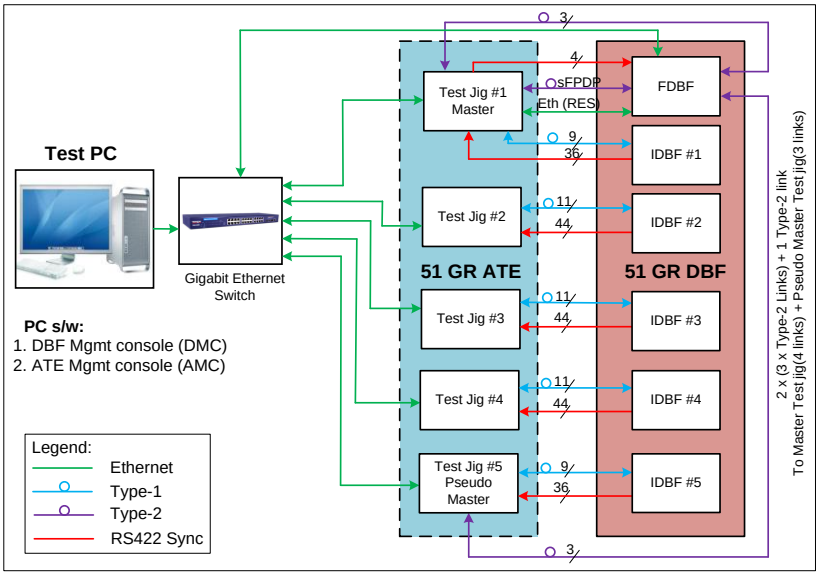

Figure 2: 51-GR DBF Test Setup

VI. Test-Jig Card and FPGA Design

Test-Jig card and FPGA block diagram is shown in Figure 3. Test Jig FPGA supports functionality to emulate surrounding systems of DBF (namely GR, STM and SP).

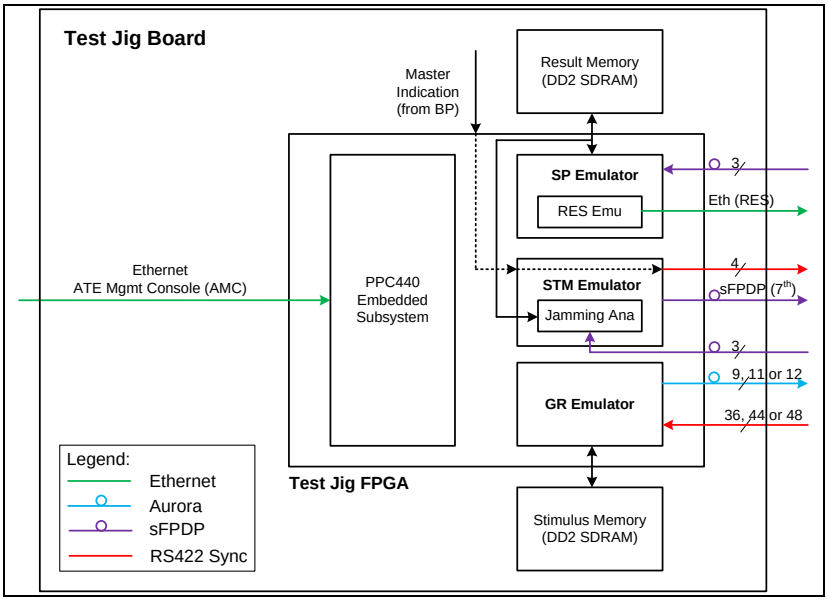

Figure 3: Logical Block Diagram of Test-Jig Card and FPGA

VII. System Operation

ATE emulates peripherals of DBF system – behaves as GRs which provide data to DBF system for beam computation; and as STM/SP which receive the computed beam from DBF.

The module emulating the Radar input data to DBF fetches packets from the stimulus memory and forwards them on high speed serial optical links to DBF. The start of transmission of packets from the stimulus memory is synchronized across multiple FPGAs and Cards. ATE can be programmed to transmit a set of packets in multiple loop mode or infinite loop mode. Infinite loop mode feature is used for regression testing of DBF.

Data is received from DBF on 6 optical links each operating at 2.5Gbps. The module behaving as SP compares received data with expected data programmed in result memory. Even a single bit error is captured and reported by ATE. ATE also supports sending RES packet on a separate 1Gbps Ethernet link to test RES functionality of DBF. ATE receives stimulus and expected result data, on separate Ethernet link connected to PC, which are programmed into stimulus and result DDR2 SDRAM memories respectively. Each packet contains generic header which can be configured to control various parameters like “inter packet delay”, “loop count”, “drop packet”, “insert CRC error”, etc.

The embedded processor based sub-system can configure the ATE either in “log mode” or “compare and log mode”. In compare and log mode, packets received from DBF are compared with the packets written in result DDR2 memory in PPC440 Embedded Subsystem caters for configuration control and status monitoring.

RTL during run time. In log mode, all the received packets are written to DDR2 memory, which can be presented to user and processed offline for errors or beam plotting. ATE supports software controlled transmit/receive buffers and internal/external loopback mechanisms. Using these features, ATE can be fully tested without requiring separate test equipment.

Using above approach, ATE has been realized for testing “24 Receiver Group DBF” and “51 Receiver Group DBF”. Using a single ATE, all the expected Receivers/SP scenarios and error scenarios have been emulated to fully validate the DBFs. MatLab simulated data has been cross verified with DBF generated data using the “log mode” of ATE.

VIII. Processor Sub-systems

Xilinx’s Virtex-5 FXT series of FPGAs come with Power PC 440 embedded processor. These embedded processors are seamlessly integrated with other essential components of an embedded sub-system such as Trimode Ethernet MAC core, dedicated DMAs, integrated crossbar, DDR memory controller etc. Using Embedded Developers’ Kit from Xilinx, processor based embedded sub-system was implemented on all the FPGAs. On board facilities essential for operation of the embedded sub-systems were provided such as Flash memories, DDR2 memories, Console port, I2C EEPROM etc.

IX. OS & Application Software

While RTL implementation is well suited for repetitive high throughput data generation and comparison tasks, it lacks the flexibility and programmability in comparison to Processor

based software implementation approach. ATE like complex systems have numerous configuration, control and status monitoring tasks that are performed at regularly in a periodic manner. Power on Self Test (POST), support for observing the health of the system, remote upgradability of FPGA images, status monitoring etc. are provided by the software.

Power PC based embedded sub-system and associated peripherals provide a great infrastructure for software implementation of these tasks. ATE architecture makes use of this.

X. System Summary

Table 1: ATE System overview

Parameter	
Number of FPGAs in ATE	15
Linux running on	5 FPGAs
BITE implementation on	5 dedicated FPGAs
Data path frequency	180MHz
Total number of optical links	80
Optical link speed	3.6 Gbps
Number of sFPDP links	20 @ 2.5 Gbps
Number of different cards in ATE	1

Table 2: FPGA resource utilization

	FDBF
Device	XC5VFX 100T -1
Clocks in MHz	90, 100,125, 180,200
FF utilization	75%
LUT utilization	69%
Slice utilization	99%
BRAM utilization	88%
GTX utilization	100%

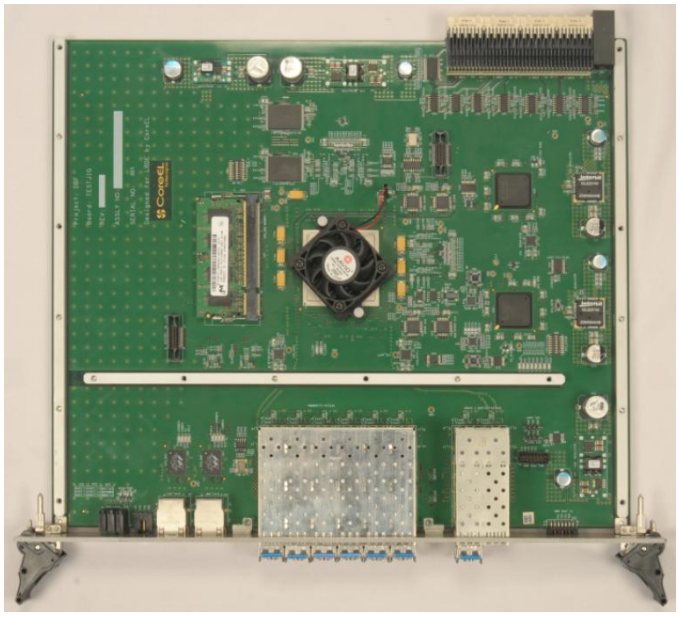

Figure 4: Test-Jig Board Photograph

XI. Conclusions

DBF system has been tested extensively in the lab using ATE for different scenarios and the results have met the design specifications in terms of functionality and throughput requirements.

Timely and successful implementation of the ATE system that requires multi-disciplinary expertise and co-ordination among teams has been possible due to proper planning, consistent adherence to quality control and assurance processes, reviews, adoption of best engineering practices and hard work.

Xilinx Virtex-5 FPGAs have proven to be a success for ATE applications, both in RTL performance and in I/O bandwidth for data processing and data communications.

ATE is architected to emulate multiple receivers. The current ATE is implemented across multiple cards and FPGAs, and can be easily scaled to emulate 1 to 60 Receiver Groups or more.

ATE RTL is adaptable to be used in various applications which require generation and analysis of packetized data. Although it is currently used to test DBF, it can be readily used to test a system which interfaces to surrounding systems using Aurora, sFPDP and Ethernet links. Further, it can be easily enhanced to test systems with varied configurations.

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